



Signal Types and Terminations

Introduction.

CMOS, HCMOS, LVCMOS, Sinewave, Clipped Sinewave, TTL, PECL, LVPECL, LVDS, CML... Oscillators and frequency control devices come with a range of different output buffer types and each type has its own advantages and disadvantages. The aim of this application note is to provide some background on each type and to provide advice on some approaches to terminating devices with such outputs.

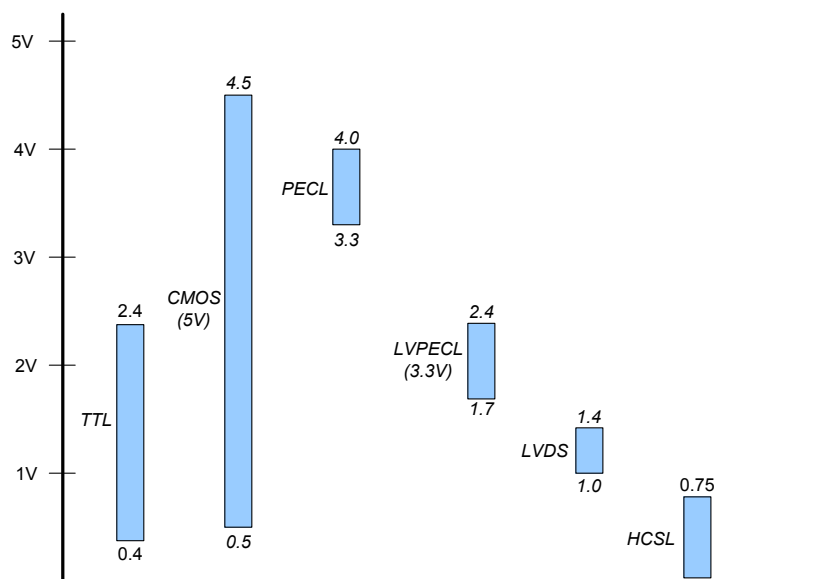


Figure 1. Approximate voltage ranges spanned by a number of common output types

The need for properly understanding signal types and terminations.

Printed Circuit Board traces behave like transmission lines that can filter a clock signal, attenuating and distorting the clock signal as it moves along the length of the trace. Higher frequency clock signals are more susceptible to attenuation, distortion, and noise, however to improve jitter clock edges with higher slew rates are preferred, creating challenges to implementing a clock solution.

To correctly implement a high quality clock source the following should be considered:

- Isolate clock sources from each other
- Utilize proper grounding and power supply filtering
- Use short PCB traces for clock signals
- Place the device to be clocked as close to the clock as possible
- Ensure that the correct clock output type has been selected for your application.
- Ensure that output drivers are terminated correctly and impedance matching techniques are employed.

The last two points are the subject of the application note. Reflections and attenuation occur when the traces are not properly terminated. Reflections will increase jitter while attenuation can further degrade the clock waveform and overall performance. Maintaining signal integrity is paramount in realizing the performance of a low phase noise oscillator.

Single Ended Output Families

Sinewave and Clipped Sinewave

Sinewave outputs are the 'natural' output of a crystal oscillator circuit and usually they represent the maximum level of spectral purity that one can expect from an oscillator. By definition a pure sine wave has only a single or fundamental frequency – and with, in the ideal case, no harmonics present. There is no 'standard' output level associated with sinewave outputs as there is in the case of the other output types, with the wave form of a sine input defined (for a given frequency) by the amplitude alone, usually

expressed as output power in dBm. Sinewave outputs are meant to drive 50 ohm impedance loads and the PC trace should also be designed to a 50 ohm impedance. Most logic output sources are derived from a sine or clipped sine wave source which degrades the phase noise performance - a sine-wave output is the ideal for demanding low phase noise applications.

Clipped sinewaves are formed by limiting a sinewave output, 'squaring off' the wave at its maximum and minimum extent. Limiting a sine wave in this way introduces additional harmonics, reducing the spectral purity of the waveform, but can offer a means to take advantage of the fast rising and falling edges in systems that cannot tolerate the full swing of a large amplitude sinewave. Clipped sinewave devices draw less power than full digital logic outputs and for this reason are popular in TCXO designs, where the additional power dissipation of a CMOS stage would influence the thermal gradients in the IC. Clipped sinewave TCXO's are meant to drive a 10pF 10K load.

CMOS, HCMOS and LVCMOS

CMOS is an acronym for Complementary Metal Oxide Semiconductor, which means that the Device (buffer) has been constructed of both p-channel and n-channel transistors.

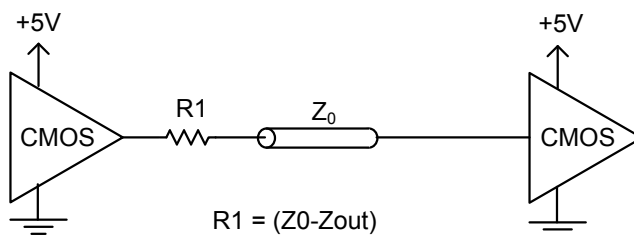
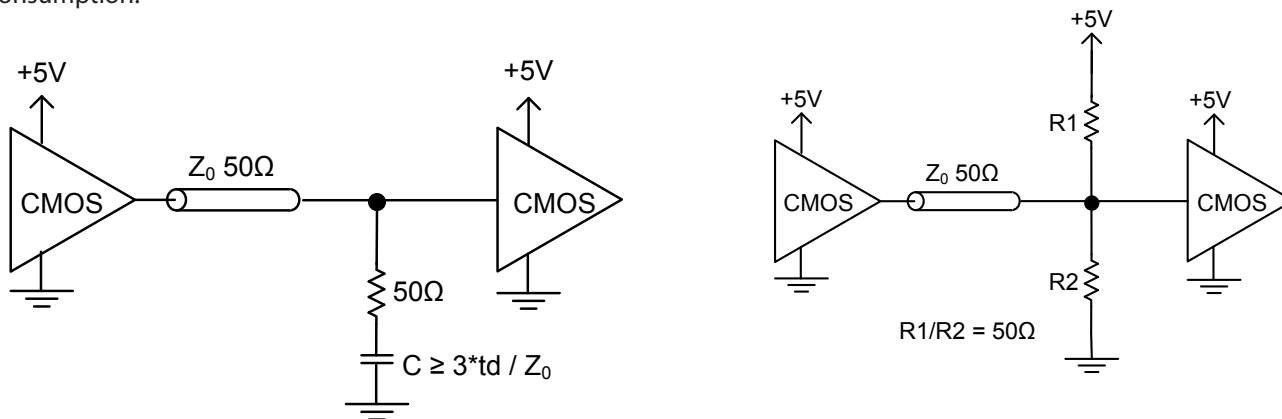


Figure 2. The most common approach to terminating a CMOS driver, suitable for short trace lengths

CMOS signals are distributed across a backplane having 50 ohm impedance traces, into one or more high impedance receivers. As such, there is an impedance mismatch. There are ways to deal with this impedance match, but between this and the inherent limits of the "rail to rail" swing, CMOS outputs are suitable for lower frequency clock sources (below 200MHz) and shorter trace lengths (less than 1/4th the wavelength of the highest harmonic frequency) that are less susceptible to impedance matching issues. For lower frequencies and short traces, a direct connection between the clock output and receiver's input can be used. But in most cases, a low value, eg 20-50 ohm, series resistor will be used which is quite effective in reducing reflections and maintaining signal integrity. See figure 2. Other methods for impedance matching are shown in figure 3 and 4, but these increase power consumption.



Figures 3 and 4. Alternative approaches to terminating CMOS

HCMOS stands for High Speed CMOS and is a higher speed variant on the original CMOS – the terms HCMOS and CMOS are often interchangeable in the oscillator world. LVCMOS stands for Low Voltage CMOS and as its name suggests it is a low voltage class of CMOS. ACMOS stands for 'Advanced CMOS'. As these acronyms are often used interchangeably, Vectron suggests specifying an oscillator using rise/fall time, output drive or load requirements and Voh/Vol as opposed to defining the requirements by the terms CMOS, HCMOS, ACMOS, LVCMOS etc.

TTL

Transistor to Transistor Logic (TTL) used to be one of the most common I/O standards. TTL operates from a +5V or 3.3V power

supply and at one time had higher transmit speeds compared to CMOS, up to 100 MHz. Also it was more popular since power consumption didn't change as drastically with higher output frequencies. TTL outputs can also be dealt with using methods described for CMOS signals. During the 1980's CMOS devices became more popular, particularly for large scale integration because of their low (zero) quiescent current, good noise immunity, improved rise/fall times and lower cost of manufacture. CMOS has displaced TTL as the preferred choice for low frequency clocking IC's.

The primary benefits of CMOS and TTL are low power consumption, higher output swing, and relatively low cost implementation in silicon. However, differential signals are used for higher frequencies.

Differential Logic Families

Single ended signal transmission techniques can be susceptible to noise. This can be overcome by increasing the voltage, but this increases the power consumption and results in lower speeds due to the voltage swing. Single ended transmission lines also tend to attenuate the signal; again this can be overcome by increasing the transmission voltage. Differential buffers overcome these difficulties by transmitting a pair of complementary signals (opposite polarities) for every bit sent. The receiver detects differences between the two signals and any noise common to both signals is rejected. Differential transmission techniques are influenced less by line attenuation because of their greater noise immunity and because of this are ideal for transmitting at higher data rates over longer line lengths.

ECL (single ended or differential)

Emitter Coupled Logic (ECL) was introduced as an alternative to TTL logic because it is better suited for high speed data transmission. Emitter-Coupled Logic circuits use transistors to steer current through gates which compute logical functions. Because the transistors are always in the active region, they can change state very rapidly, so ECL circuits can operate at very high speeds.

ECL suffers from two disadvantages. First, ECL requires relatively high currents to operate. Secondly, ECL relies on a negative power supply for operation. This can cause problems when interfacing to positive-supply-based devices residing in the rest of the system. But being referenced to ground, could offer noise advantages

PECL, LVPECL

LVPECL and PECL are both offshoots of the older ECL technology first introduced in the 1960s. PECL stands for Positive Emitter Coupled Logic as it operates off a positive voltage such as 5, 3.3V or 2.5V. PECL logic outputs are commonly used in high-speed clock distribution circuits. As a differential transmission scheme PECL has the advantage of high noise immunity and the ability to drive high data rates over long line lengths. Another advantage of PECL includes good jitter performance due to the large voltage swing. Disadvantages include large power consumption (compared to a single ended supply) due to the need for a 5V supply and external DC biasing.

Low Voltage PECL (LVPECL) refers to PECL circuits designed for use with 3.3V or 2.5V supply, the same supply voltages as for low voltage CMOS devices. LVPECL forms the basis of a number of protocols including Gigabit Ethernet and Fibre Channel. The LVPECL electrical specification is similar to LVDS, but operates with a larger differential voltage swing. LVPECL tends to be a little less power efficient than LVDS due to its ECL origins and larger swings, however it can also operate at frequencies up to 10 Gbps because of its ECL characteristics.

LVPECL output currents are typically 15mA, and this is derived from an open emitter. This requires termination into a resistive load to produce a voltage. The intent for LVPECL is to use a 50 ohm impedance trace and 50 ohm thevenin equivalent load. This is usually implemented using figure 5 and an alternative scheme is shown in figure 6. For best performance, the outputs should be equally terminated using the same method - an unused output should never be left floating. Also differential receivers from different manufacturers can have different input tolerances (while still clustered around a common standard). Doing some homework on the requirements of the receiver can also help to optimize the transmission of the signal you are looking to terminate.

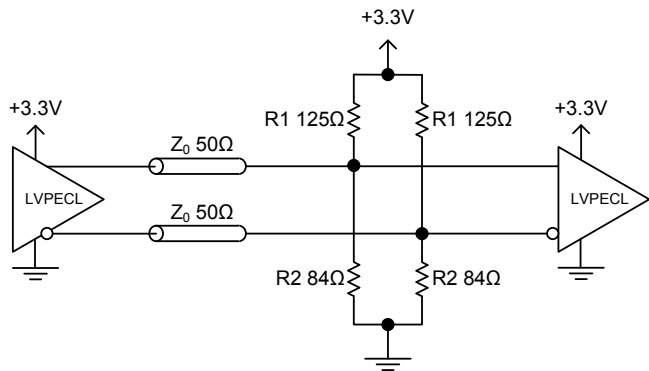


Figure 5. The most common approach to LVPECL termination

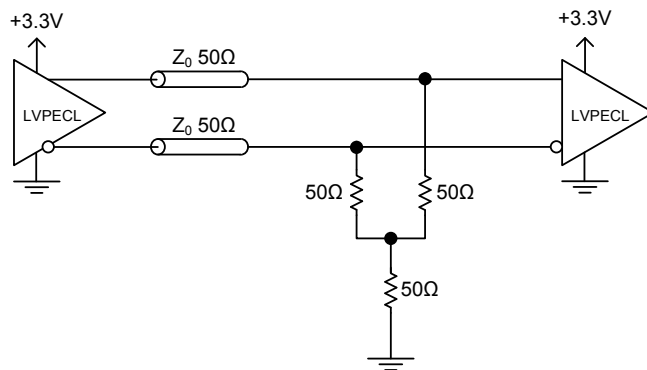


Figure 6. An alternative LVPECL termination scheme

CML

Current-Mode Logic (CML) outputs provide similar performance to LVPECL but do not require an external bias and so CML is an option when an LVPECL type output is required but power consumption is a concern. CML outputs need to be ac-coupled since they cannot provide sufficient current to bias other devices.

LVDS

LVDS stands for Low Voltage Differential Signaling, and is similar to LVPECL being a current output, however the output current is 4mA which results in lower power consumption compared to LVPECL. LVDS outputs have a 100 ohm output impedance and is meant to drive a 100 ohm load or resistor, this results in smaller voltage swings typically ~350mV.

LVDS maintains reduced susceptibility to noise, lower EMI emissions compared to CMOS and TTL. A disadvantage of LVDS can be its reduced jitter performance compared to PECL; however advances are being made putting it on a level playing field with LVPECL.

LVDS is used in high speed data transfer applications, in particular backplane transceivers or clock distribution. LVDS operates at data rates up to 3.125 Gbps. For higher data rates, outputs such as HCSL, CML or LVPECL are required. Achieving these very high data rates requires very fast, sharp-edge rates and typically a signal swing of approximately 800 mV. Because of this HCSL, CML and LVPECL generally require more power than LVDS.

LVDS is typically chosen for newer designs because of its ease of implementation in CMOS ICs and because of ease of use at the system level. LVDS outputs require no external biasing and a single 100 ohm termination resistor when connected to LVDS inputs, see figure 7. The LVDS signal may or may not need to be AC coupled after the 100 ohm load - it's always best to understand the receiver's input structure requirements.

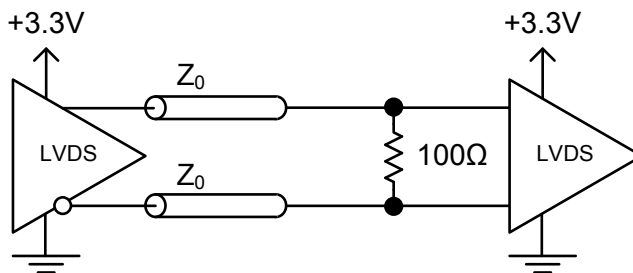


Figure 7. Terminating LVDS. Often the receiver includes on chip termination and the additional 100 ohm resistor is not required.

HCSL

High Speed Current Steering Logic (HCSL) outputs are found in PCI express applications and Intel chipsets. HCSL is a newer dif-

ferential output standard, similar to LVPECL, with a 15mA current source being derived from an open emitter or source. Being un-terminated drains, they require external 50 ohm resistors to ground as shown in in figure 8. HCSL is a high impedance output with quick switching times, in can be advantageous to use a 10 to 30 ohm series resistor as shown in Figure 9, to help reduce overshoot/ringing. HCSL provides the quickest switching speeds, power consumption is between LVDS and LVPECL, and phase noise performance compares well with the alternative technologies. As always it is best practice to understand a receivers input structure.

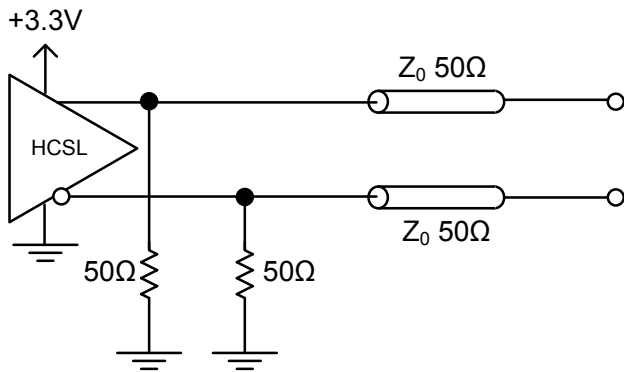


Figure 8. Single Resistor Termination Scheme

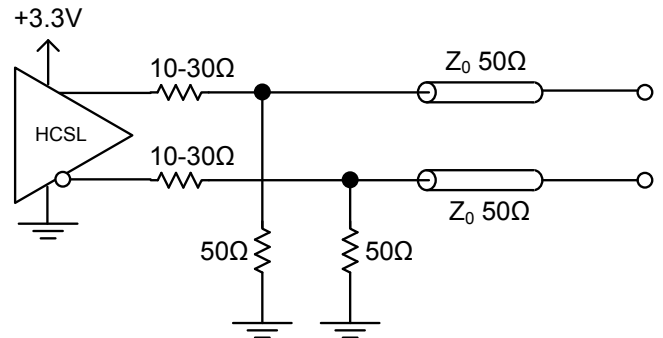


Figure 9. In some cases a 10-30 ohm series resistor is used to help reduce overshoot.

Benefits/Tradeoffs**Jitter:**

LVPECL can offer best jitter performance followed by LVDS, and then CMOS; however CMOS can usually provide better phase noise albeit slower rise and fall times resulting in degraded jitter in some cases

Power:

For the best power consumption use CMOS or LVDS. LVPECL is faster but consumes more power

Speed:

HCSL and LVPECL is faster but can consume more power. LVDS is faster than CMOS.

Single ended vs. differential:

Differential signals are resistant to common mode noise which single ended techniques are susceptible to, and there are less EMI concerns. Additionally, differential signals have better rise and fall time. However, sinewave generally offers the best phase noise followed by CMOS then differential.

Ease of use:

LVPECL requires external resistors for termination at both transmitter and receiver ends. LVDS requires only single resistor at receiver

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